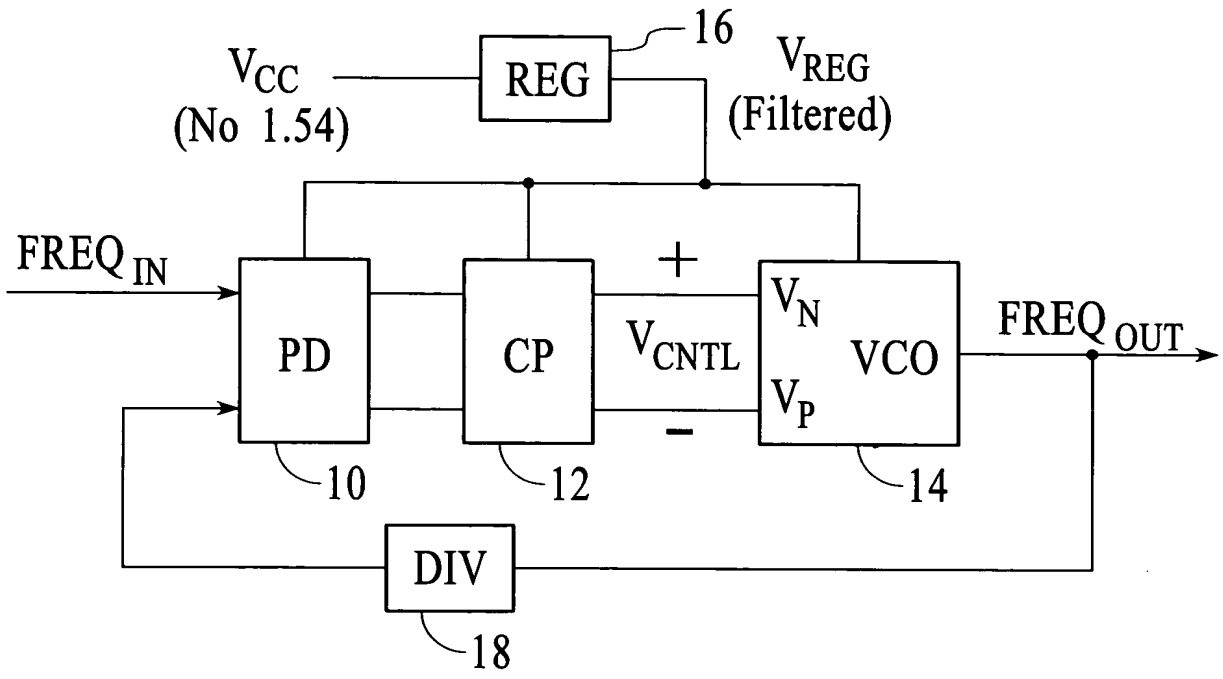

FIG. 1
(PRIOR ART)

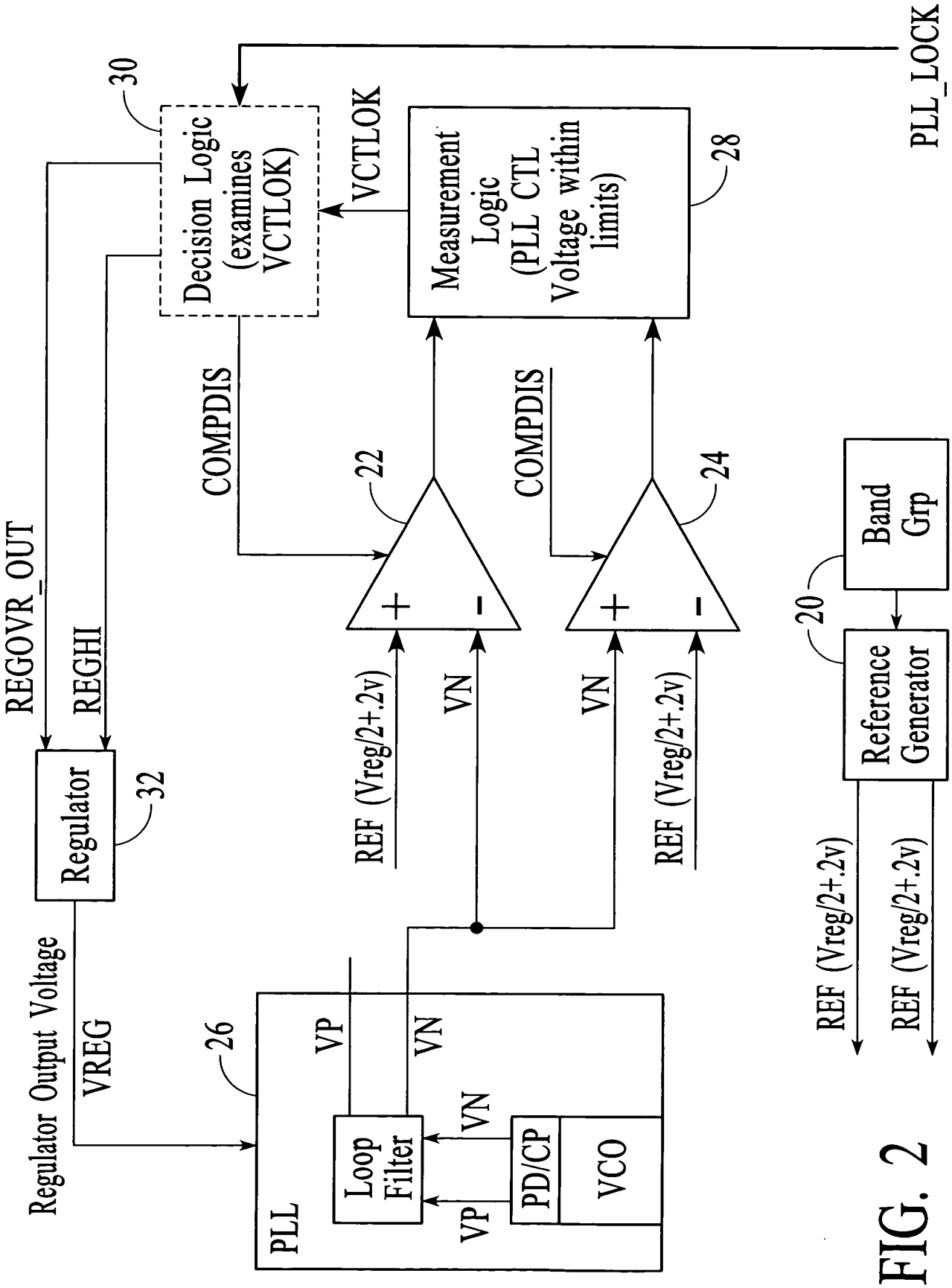
PLL_LOCK
30
Decision Logic (examines VCTLOK)
VCTLOK
Measurement Logic (PLL CTL Voltage within limits)
28
COMPDIS
COMPDIS
22
24
REGOVR_OUT
REGHI
Regulator
32
REF (Vreg/2+.2v)
VN
VN
REF (Vreg/2+.2v)
Band Grp
20
Reference Generator
REF (Vreg/2+.2v)
REF (Vreg/2+.2v)
Regulator Output Voltage
VREG
26
PLL
VP
VN
Loop Filter
VN
PD/CP
VCO
VP

FIG. 2

Table 1: REGVHI and REGOVR_OUT Mapping

REGVHI	REGOVR_OUT	Regulator Voltage
0	0	1.1V
0	1	1.2V
1	0	not allowed
1	1	1.3V

If at any time REGOVER_IN = '1' then
REGVHI = '0', REGOVR_OUT = '1', COMPDIS = '1', and BLOCK_PLLLOCK = '0'.
Else
After reset or power up:
REGVHI = '1', REGOVR_OUT = '1', COMPDIS = '0', and BLOCK_PLLLOCK = '1'.
Wait 150 us.
Sample (VCTLOK ended with internal PLL_LOCK indicator).
If VCTLOK_SAMPLE = '1' then
REGVHI = '1', REGOVR_OUT = '1', COMPDIS = '0', and BLOCK_PLLLOCK = '0'.
Stop. Keep outputs the same until next reset.
Else
REGVHI = '0', REGOVR_OUT = '0', COMPDIS = '0', and BLOCK_PLLLOCK = '1'.
Wait 150 us.
Sample (VCTLOK ended with internal PLL_LOCK indicator).
If VCTLOK_SAMPLE = '1' then
REGVHI = '0', REGOVR_OUT = '0', COMPDIS = '1', and BLOCK_PLLLOCK = '0'.
Stop. Keep outputs the same until next reset.
Else
REGVHI = '0', REGOVR_OUT = '0', COMPDIS = '1', and BLOCK_PLLLOCK = '1'.
Stop. Keep outputs the same until next reset.
End if

FIG. 3